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REMARKS

Claims 1-9, 11-20 and 23-114 are pending in this application. Claims 4, 24-34, 45-54, 59-71 and 78-93 stand withdrawn from consideration as being directed to a non-elected invention or species of invention. Claims 2, 3, 5-9, 11-14, 17, 36, 38-44, 57, 58, 99, 103 and 110 have been deemed to present allowable subject matter and would be allowed if presented in independent form. The specification and claims 35 and 37 have been objected to, and claims 1, 15, 16, 18-20, 23, 35, 37, 55, 56, 72-77, 94-98, 100-102, 104-109 and 111-114 have been rejected. Claims 1, 15, 35, 55, 72, 98, 100, 108 and 114 (and withdrawn claims 26, 45, 47, 78, 87 and 89) are independent.

By this Amendment Applicants seek to amend claims 1, 15, 35, 55, 72, 97, 100-102, 105, 107-109, 112 and 114. Upon entry of this Amendment, claims 1, 15, 35, 55, 72, 98, 100, 108 and 114 (and withdrawn claims 26, 45, 47, 78, 87 and 89) will remain independent.

It is respectfully submitted that because the claim amendments involve issues already considered by the Examiner, this Amendment can be entered without any substantial new work. It is further submitted that all outstanding rejections are overcome by the arguments set forth below.

The Examiner is thanked for the indication of allowable subject matter in claims 2, 3, 5-9, 11-14, 17, 36, 38-44, 57, 58, 99, 103 and 110. Those claims have been maintained unchanged, since, as explained below, the claims from which they respectively depend are themselves allowable over the art of record.

The Examiner is also thanked for the telephonic interview conducted on April 8, 2003. Generally, the claims have been revised in accordance with the discussion between the Examiner and Applicants' undersigned attorney during that interview.

The Objection to the Specification

The specification was objected to as failing to provide a proper antecedent basis for certain claimed subject matter. Specifically, the Office Action stated that the language in claim 99 providing that the second memory area is located at a first half of an entire memory space of the non-volatile sequential access memory is not supported by the specification.

As explained during the aforementioned telephonic interview, this aspect of the present invention is supported by Figures 8 and 19, and the corresponding portions of the specification. In this regard, the disclosure at pages 37 and 54 has been revised to discuss what would be apparent to those skilled in the art from Figs. 8 and 19, namely, that first storage area constitutes one half of the memory cell and the second storage area constitutes the other half of the memory cell.

Accordingly, the specification now more than sufficiently supports the claim feature in question. As explained during the telephonic interview, the revisions to the specification do not raise issues of new matter because they simply describe what those skilled in the art would recognize from the drawings as filed.

For all the foregoing reasons, favorable reconsideration and withdrawal of this objection is respectfully requested.

The Objection to the Claims

Claims 35 and 97 were objected to on grounds certain claim language required correction. The Examiner helpfully suggest changes that would overcome these objections. Applicants thank the Examiner for those suggestions.

Claims 35 and 97 have been revised along the lines suggested by the Examiner. Accordingly, favorable reconsideration and withdrawal of these objections is respectfully requested.

The Rejection Under 35 U.S.C. § 102

Claims 1, 15, 16, 18-20, 23, 35, 37, 55, 56, 72-77, 94-96, 100-102, 104-109 and 111-114 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,610,635 to Murray et al. Applicants respectfully traverse this rejection and submit the following arguments in support thereof.

As discussed during the telephonic interview, various claims have been revised to clarify the aspects of this invention relating to the timing (and/or location) of reading and/or writing information into the sequential access memory device. It should now be clear that the "static" information such as ink color, which need not be changed during operation, is located in a portion of the memory that takes longer to access than the portion where the "dynamic" information that changes during operation, such as the amount of ink remaining, is stored.

It should be noted that, as explained during the telephonic interview, the claims provide for the use of sequential access memory (the rejected independent claims will be described in detail later in this response). As is well-known in the art, sequential access memory

differs from random access memory in that information stored in sequential access memory must be retrieved or written in an ordered, successive manner, progressing from the first storage location to the last storage location. In contrast, when random access memory is used, information can be directly retrieved from or written to a particular memory location of interest, without having to go through the preceding memory locations, which may be faster.[1] Random memory access however, is typically more expensive than sequential access memory, meaning that when choosing a type of memory, there will be a trade-off between performance and cost.

Sequential access memory is different from random access memory. As evidence supporting this distinction between sequential access memory and random access memory, Applicants submit herewith a webpage entitled "Random vs. Sequential Access Memory"[2] from the website "http://howto.lycos.com" which explains that information is retrieved from or written to sequential access memory in stepwise fashion". The accompanying webpage entitled "Random Access Memory"[3] from the website "http://www.pcguide.com" also distinguishes sequential access memory from random access memory. Likewise, U.S. Patent No. 3,991,409 to Dautremont, Jr. et al. distinguishes sequential access memory from random access memory (col. 4, lines 49-53). All of these materials are being cited in accordance with M.P.E.P. § 609 (III)(C)(3). The Examiner is respectfully requested to confirm that these materials have been considered.

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1 During the interview on April 8, 2003, the Examiner made a number of comments indicating the Examiner did not appreciate that sequential access memory, as claimed, operates in a different manner than random access memory. In fact, the Examiner indicated he did not understand why access time for serial (sequential) memory depends upon the position of the memory address being accessed. Accordingly, Applicants will first address this aspect of the present invention.

2 Webpage URL: http://howto.lycos.com/lycos/step/1,,5+26+74+26288+10254,00.html

3 Webpage URL: http://www.pcguide.com/ref/ram/typesRAM-c.html

These references establish that one skilled in the art will recognize that sequential access memory and random access memory are not the same, and that in sequential access memory, the time required to read from or write to a specific memory location depends upon the position of that location in the sequential access memory. Accordingly, it is understood that when using sequential access memory, the position of the memory location being read from or written to affects the access time for the information of interest. A memory location near the beginning of the memory can be accessed faster than a memory location at the end of the memory.

During the telephonic interview, the undersigned explained why the claimed invention confers benefits not available in the art of record, and the Examiner invited Applicants, when responding to the Office Action, to point out where in this application such benefits are discussed.

Moreover, one aspect of the present invention is that the ink quantity information storage area is located at a specific area that is the area located within the sequential access storage unit that is accessed for rewriting by the printer first before accessing for rewriting any other area within the sequential access storage unit where another type of information is stored. As explained during the interview, rewriting this information at a position before the position where other rewritable data is stored can confer operational benefits.

In response to the Examiner's invitation, Applicants call attention to the following portions of this application (these portions are identified by way of example only and not limitation, and other portions of the application also may be germane to the Examiner's invitation).

By way of example only and not limitation, Figs. 13B, 29 and 30, and the discussion from pages 41-43 and 68-70 of the specification describe how information is loaded into specific storage areas (660 or 760) of the sequential memory / storage elements 80. Likewise, at page 5, first full paragraph, and page 36, least full paragraph, there are discussions of how the location where the ink quantity information is stored affects access time.

The specification at pages 43-45 and 70-71 recognizes the benefits that are obtained by storing information as claimed (where the memory location of the dynamically-changing ink quantity information is accessed more quickly). Among such benefits are faster storage of the information being recorded, which reduces the likelihood that such information will be lost if power is interrupted during recording of that information (page 44 and 70-71)

As noted in detail below, the claimed invention provides in each case for the use of sequential access-type memory.

According to claim 1, this invention relates to an ink cartridge that can be detachably attached to a printer. The ink cartridge has an ink reservoir where ink is kept and a **sequential** access storage unit storing specific information in a readable, writable, and non-volatile manner. The specific information includes an ink quantity-relating information relating to a quantity of ink kept in the ink reservoir and the storage unit is sequentially accessed in synchronism with a clock signal, and has an ink quantity information storage area storing the ink quantity-relating information. The ink quantity information storage area is located at a specific area that is the area located within the sequential access storage unit that is accessed for rewriting by the printer first before accessing for rewriting any other area within the sequential access storage unit where another type of information is stored.

As set out in claim 15, this invention also involves an ink cartridge configured to be detachably attached to a printer. This ink cartridge has an ink reservoir that keeps ink used for printing, and a **sequential** access storage unit storing information in a readable, writable, and non-volatile manner and which is sequentially accessed in synchronism with a clock signal. The storage unit has a first storage area, in which read only information is stored, and a second storage area, which is the area located within the storage unit that stores rewritable information relating to a quantity of ink kept in the ink reservoir and is accessed for rewriting by the printer first before accessing for rewriting any other area within the storage unit.

Applicants' invention, as defined in claim 35, pertains to a method of writing plural pieces of specific information into an ink cartridge, this ink cartridge having been configured to be detachably attached to a printer and having a **sequential** access storage element. The method includes the steps of (a) receiving the plural pieces of specific information that are to be written into the storage element by the printer, wherein the plural pieces of specific information comprises information relating to a quantity of ink kept in the ink cartridge and other information, and (b) rewriting the ink quantity-relating information into the storage element preferentially over the other pieces of specific information at an area within the storage element that is the area located within the storage element that is accessed for rewriting first before accessing for rewriting any other area within the storage element.

Claim 55 provides for an ink jet printer having an ink cartridge that is detachably attached to a printer main body and in which ink is kept. The printer main body causes the ink kept in the ink cartridge to be ejected from a print head onto a printing medium, so as to implement printing on the printing medium. The ink cartridge includes a **sequential** access type storage device which has a storage unit and an address counter that carries out either a count-up

operation or a count-down operation in response to a clock signal in the course of data transmission between the storage unit and the printer main body. The storage unit included in the storage device has a first storage area, in which read only data are stored and which is only read by the printer main body, and a second storage area, in which rewritable data are stored and which is the area located within the storage device that is accessed for rewriting by the printer first before accessing for rewriting any other area within the storage device. The ink jet printer also has a data input-output unit that carries out reading and writing operations in response to a clock signal.

As recited in claim 72, Applicants' invention also concerns a storage device mounted on an ink cartridge which is configured to be detachably attached to a printer. The storage device has an address counter that outputs a count in response to a clock signal output from the printer and a storage element that is **sequentially** accessed based on the count output from the address counter, and which has a storage area where plural pieces of specific information are stored in a readable, writable, rewritable and non-volatile manner at an area storing the specific information and located within the storage element that is accessed for rewriting first by the printer first before accessing for rewriting any other area within the storage element. The specific information relates to a quantity of ink kept in the ink cartridge.

Applicants' invention, as set out in claim 98, is drawn to an ink cartridge configured to be detachably mountable on a printer, and which includes an ink reservoir for keeping ink and a non-volatile sequential access memory that is **sequentially** accessed from an access start position in synchronism with a clock signal, the memory having a first memory area for storing data not to be updated according to use of the ink cartridge and a second memory area for storing data to be updated according to use of the ink cartridge. The second memory area has

a specific area for storing ink quantity data related to consumption of the ink, the specific area being located at a front end of the second memory area which is to be written first in writing data to the second memory area.

As set out in claim 100, the present invention also is directed to an ink cartridge configured to be detachably attached to an ink-jet printer. The cartridge has an ink storage reservoir and a non-volatile **sequential** access storage element that stores data. The storage element has a first storage area for storing read-only data, and a second storage area for storing rewritable data at pertaining to ink-quantity related information. The second storage area is accessed for rewriting by the printer first before accessing for rewriting any other area within the storage element.

Applicants' invention, as described in claim 108, also involves a method of providing a data in an ink cartridge that is configured to be detachably mountable on a printer, the ink cartridge having a non-volatile **sequential** access memory, through the steps of, first, storing read-only data in a first storage area of the memory. The second storage area is accessed for rewriting by the printer first before accessing for rewriting any other area within the memory.

Claim 114 relates to a method of retrieving data from an ink cartridge that is configured to be detachably mountable on a printer. The ink cartridge has a non-volatile **sequential** access memory, and the memory contains read-only data at a first address and rewritable data at a second address in the memory. The second address is closer to a beginning of the storage device than the first address. This method includes the step of reading the second data without reading the first data.

Bearing in mind the use of sequential type memory in the claimed invention, it will be appreciated that there are substantial and important differences between the claimed

invention and the teachings of Murray. Accordingly, Murray does not identically disclose, or even suggest, all the features of each of the rejected claims.

Although Murray discloses an ink cartridge which that has a memory for storing information, and in one case stats the memory is random access, Murray does not state that a sequential access memory is used (see col. 6, lines 39-60).

The Office Action correctly notes that Murray teaches the use of EEPROM memory (Office Action, pp. 3-4); however, Applicants respectfully wish to point out that the EEPROM memory is not necessarily sequential-access memory, as is claimed. Further, there is no explanation in Murray how Murray's EEPROM memory is accessed. See col. 6, lines 39-60.

While Applicants have not been able to determine whether Murray's EEPROM memory is sequential access memory, the Applicants have determined that the type of memory which Murray discloses as an example, model DS 1220AB/AD by Dallas Semiconductor, is not a sequential access memory. As evidence that the Dallas Semiconductor memory does not operate this way, Applicants submit herewith a product specification sheet for this model of memory.

Accordingly, Murray does not teach this aspect of Applicants' invention, and so, for this reason alone, Murray does not anticipate or even suggest the present invention.

Even assuming, *arguendo*, one skilled in the art were to interpret Murray to cover use of a sequential access memory (and Applicants do not concede this point), Murray still does not describe how the information is arranged in that memory, much less arranging such information in the manner claimed.

Although the Office Action asserts that Murray teaches an ink quantity information storage area storing the ink-quantity relating information as a "storage area of 48"

(Office Action, p. 4), still does not suggest the present invention. Murray just teaches that certain types of information regarding the ink cartridge are stored in memory element 48, but does not suggest that of the different types of information stored in the memory element, one type of information is stored in a particular location relative to the other types of information. See col. 6, line 38, through col. 7, line 10; col. 8, line 34, through col. 10, line 17; and col. 12, line 64, through col. 13, line 35.

In other words, even if Murray suggests using a sequential access memory to store different types of information about the ink in the cartridge, Murray still does not teach those skilled in the art to store the information so that dynamic information which changes in value over time, like the amount of ink remaining, is located in portion of the memory which can be accessed most rapidly, ahead of other types of information, as is done in the present invention.

Since Murray does not suggest this aspect of Applicants' invention, that invention patentably distinguishes over Murray.

The remaining rejected claims, claims 16, 18-20, 23, 37, 56, 73-77, 94-96, 101, 102, 104-107, 109 and 111-113, all ultimately depend from and so incorporate by reference all the features of the foregoing independent claims, including those features just shown to avoid the cited art. These dependent claims are therefore patentable over the cited art at least for the same reasons as their respective parent claims.

For all the foregoing reasons, favorable reconsideration and withdrawal of this rejection are favorably requested.

The Rejection Under
35 U.S.C. § 103

Claim 97 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Murray. Applicants respectfully traverse this rejection and submit the following arguments in support thereof.

Claims 97 depends from claim 1, and so incorporates by reference all the features of claim 1, including those features previously shown to avoid Murray.

For all the foregoing reasons, favorable reconsideration and withdrawal of this rejection is respectfully requested.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Applicants submit herewith for the Examiner's consideration copies of a webpage entitled "Random vs. Sequential Access Memory"[4] from the website "http://howto.lycos.com" and a webpage entitled "Random Access Memory"[5] from the website "http://www.pcguide.com", as well as U.S. Patent No. 3,991,409 to Dautremont, Jr. et al.

In accordance with M.P.E.P. § 609 (III)(C)(3), a Statement under 37 C.F.R. § 1.97(e) has not been provided.

Pursuant to M.P.E.P. § 609 (III)(C)(3), the Examiner is respectfully requested to confirm that these references have been considered.

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[4] Webpage URL: http://howto.lycos.com/lycos/step/1,,5+26+74+26288+10254,00.html

[5] Webpage URL: http://www.pcguide.com/ref/ram/typesRAM-c.html

CONCLUSION

The Commissioner is authorized to charge any fees now or hereafter due in connection with the prosecution of this application to Deposit Account No. 19-4709.

Applicants respectfully submits that all outstanding objections and rejections have been addressed and are now either overcome or moot. Applicants further submit that all claims pending in this application are patentable over the prior art. Favorable reconsideration and withdrawal of those rejections and objections is respectfully requested.

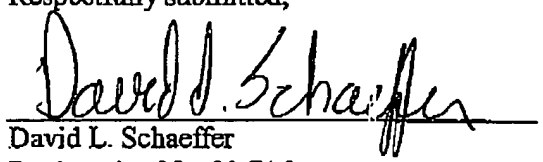
In view of the foregoing revisions and remarks, Applicants respectfully request entry of this amendment and submit that entry of this amendment will place the present application in condition for allowance. It is further submitted that entry of this amendment can be approved by the Examiner consistent with Patent and Trademark Office practice, since the changes it makes should not require a substantial amount of additional work by the Examiner. It is believed that the changes presented in this amendment either address matters of form or issues that the Examiner has previously considered.

Favorable consideration and prompt allowance of this application is respectfully requested. In the event that there are any questions, or should additional information be required, please do not hesitate to contact Applicants' attorney at the number listed below.

Applicants have made a diligent effort to place the application in condition for allowance and respectfully submit that the claims as now presented are in condition for immediate allowance. If, however, the Examiner feels he cannot issue an immediate Notice of

Allowance, the Examiner is respectfully requested to contact the undersigned attorney to discuss the outstanding issues.

Respectfully submitted,



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資料 12

DALLAS SEMICONDUCTOR MAXIM

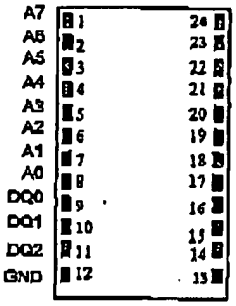
www.maxim-ic.com

DS1220AB/AD
16k Nonvolatile SRAM

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 2k x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- JEDEC standard 24-pin DIP package
- Read and write access times as fast as 100 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1220AD)
- Optional ±5% V_{CC} operating range (DS1220AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



24-Pin ENCAPSULATED PACKAGE
720-mil EXTENDED

PIN DESCRIPTION

A0-A10	- Address Inputs
DQ0-DQ7	- Data In/Data Out
$\overline{CE}$	- Chip Enable
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
V_{CC}	- Power (+5V)
GND	- Ground

DESCRIPTION

The DS1220AB and DS1220AD 16k Nonvolatile SRAMs are 16,384-bit, fully static, nonvolatile SRAMs organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. The NV SRAMs can be used in place of existing 2k x 8 SRAMs directly conforming to the popular bytewide 24-pin DIP standard. The devices also match the pinout of the 2716 EPROM and the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1220AB and DS1220AD execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 11 address inputs (A0-A10) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{CE}$ and $\overline{OE}$ access times are not satisfied, then data access must be measured from the later-occurring signal and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1220AB and DS1220AD execute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{OPW} from its falling edge.

DATA RETENTION MODE

The DS1220AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5V. The DS1220AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1220AB and 4.5 volts for the DS1220AD.

FRESHNESS SEAL

Each DS1220 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1220AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1220AD Power Supply Voltage	V_{CC}	4.50	5.0	5.50	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(T_A: See Note 10)
(V_{CC} =5V ± 5% for DS1220AB)
(V_{CC} =5V ± 10% for DS1220AD)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ =2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ =V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current (Commercial)	I_{CC01}			75	mA	
Operating Current (Industrial)	I_{CC01}			85	mA	
Write Protection Voltage (DS1220AB)	V_{TP}	4.5	4.62	4.75	V	
Write Protection Voltage (DS1220AD)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(T_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

AC ELECTRICAL CHARACTERISTICS

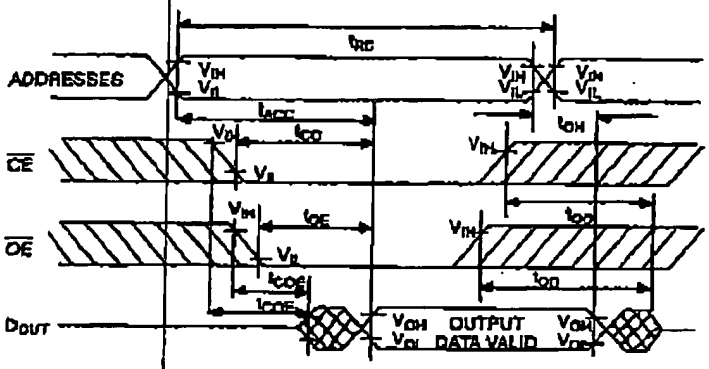
(T_A: See Note 10)
(V_{CC} =5.0V ± 5% for DS1220AB)
(V_{CC} =5.0V ± 10% for DS1220AD)

PARAMETER	SYMBOL	DS1220AB-100 DS1220AD-100		DS1220AB-120 DS1220AD-120		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	100		120		ns	
Access Time	t_{ACC}		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		120		ns	
Write Pulse Width	t_{WP}	75		90		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1}	0		0		ns	12
	t_{WR2}	10		10		ns	13
Output High from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	4
Data Setup Time	t_{DS}	40		50		ns	4
Data Hold Time	t_{DH1}	0		0		ns	12
	t_{DH2}	10		10		ns	13

AC ELECTRICAL CHARACTERISTICS (cont'd)

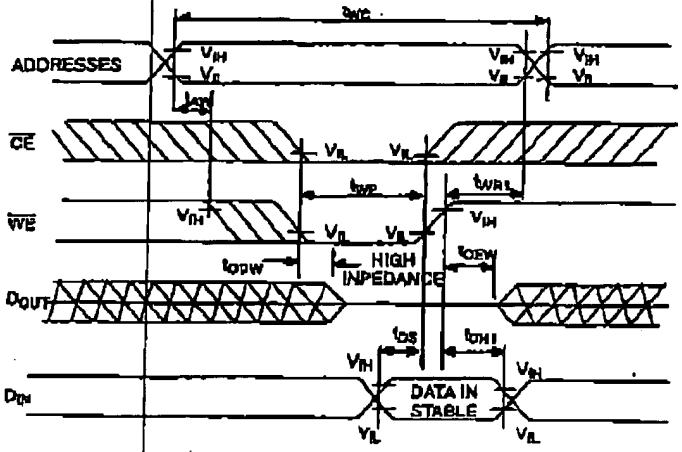
PARAMETER	SYMBOL	DS1220AB-150 DS1220AD-150		DS1220AB-200 DS1220AD-200		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		150		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1}	0		0		ns	12
	t_{WR2}	10		10		ns	13
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	4
Data Setup Time	t_{DS}	60		50		ns	4
Data Hold Time	t_{DH1}	0		0		ns	12
	t_{DH2}	10		10		ns	13

READ CYCLE



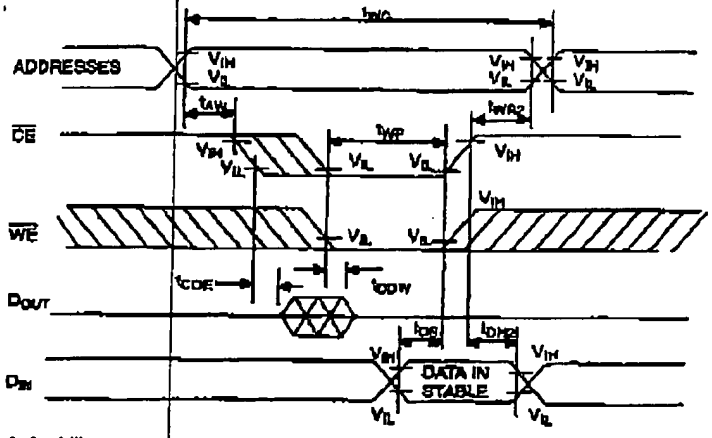
SEE NOTE 1

WRITE CYCLE 1



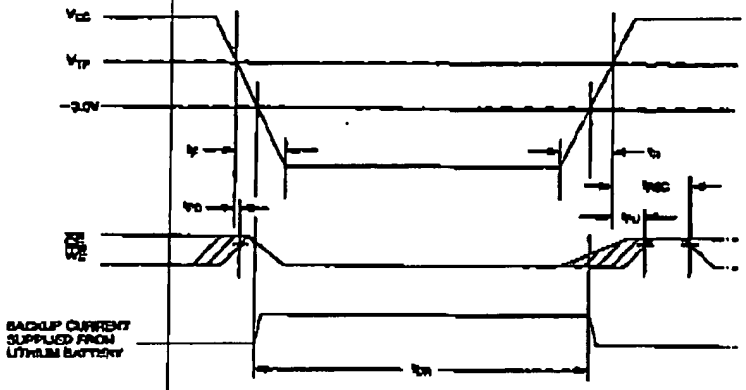
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(T_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PD}			1.5	µs	11
V_{CC} slew from V_{TP} to 0V	t_F	300			µs	
V_{CC} slew from 0V to V_{TP}	t_R	300			µs	
V_{CC} Valid to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PU}			2	ms	
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	

(T_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in the battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high-impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{CE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high-impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.

8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.
9. Each DS1220AB and each DS1220AD has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
14. DS1220 modules are recognized by Underwriters Laboratory (U.L.®) under file E99151.

DC TEST CONDITIONS

Outputs Open
Cycle = 200ns for Operating Current
All Voltages Are Referenced to Ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

ORDERING INFORMATION

DS1220 TTP – SSS – III

Operating Temperature Range
Blank: 0°C to 70°C
IND: –40°C to +85°C

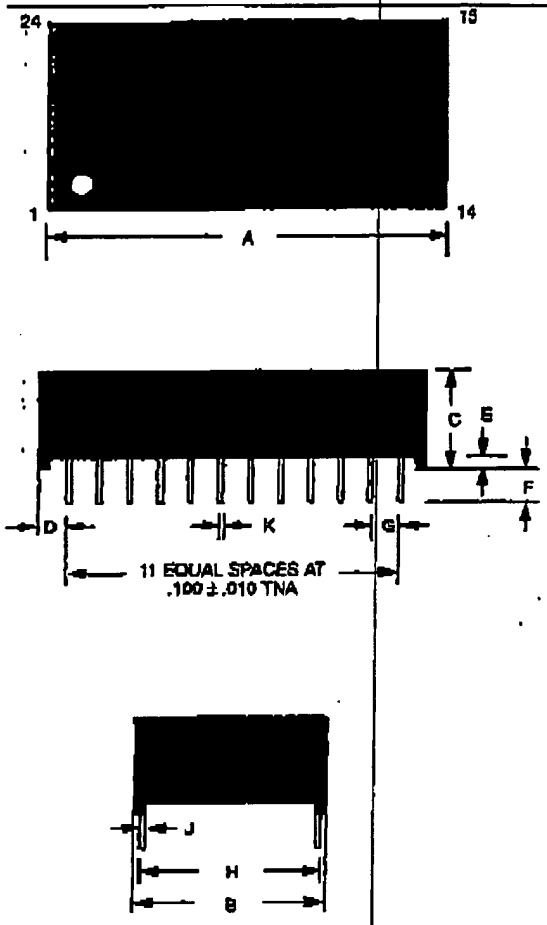
Access Speed
100: 100 ns
120: 120 ns
150: 150 ns
200: 200 ns

Package Type
Blank: 24-pin 600 mil DIP

V_{CC} Tolerance
AB: ±5%
AD: ±10%

DS1220AB/AD NONVOLATILE SRAM, 24-PIN 720-MIL EXTENDED MODULE

PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.320	1.340
MM	33.53	34.04
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.390	0.415
MM	9.91	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030



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Random vs. Sequential Access Memory

Step 1: Random Access Memory

As mentioned, the type of memory we have been discussing-that is, the memory used to temporarily house programs and data-is called random access memory, or RAM for short. To understand where this name comes from, you need to know more about how information is stored in memory.

Step 2: Sequential Access

Remember, the CPU treats memory as a set of numbered storage bins, rather like a collection of mailboxes, each one of which holds a single character. In early computers, the CPU had to access the mailboxes (bytes) in numerical order, starting from the first mailbox and moving forward until it reached the one that actually contained the desired information. This is known as sequential access. With the development of random access memory, the CPU can go directly to whichever mailbox it is interested in.

Step 3: RAM vs. Sequential Access

The difference between RAM and sequential access memory is similar to CDs vs. cassette tapes. If you want to listen to the fifth song on a cassette tape (sequential access), you have to start at the beginning of the tape and move past the first four songs. With a CD (random access), you can go directly to song five. Disks are random access devices, too. Rather than starting from the outside of the disk and reading inward, or the inside and reading outward, the read/write head can jump directly to where the data is stored.

Step 4: What is ROM?

Add to My Favorites
View My Favorites

Related Tutorials
The Brains of the Computer
Input and Output
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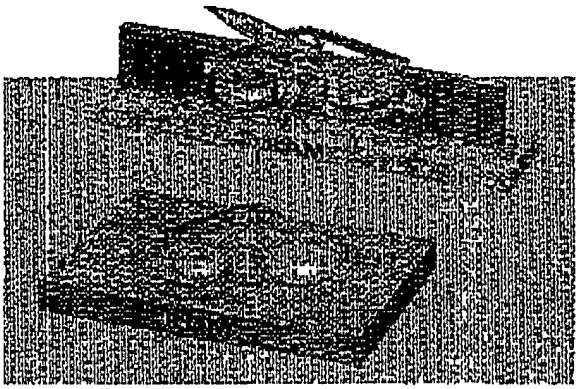
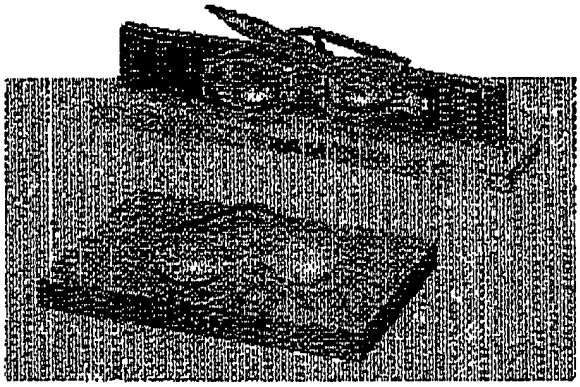
Memory: The Electronic Desktop
Load a Program into Memory
Save Data
Random vs. Sequential Access Memory
Inside the System Unit
How Memory and Disks Are Measured



There is actually a second type of memory used in personal computers, in addition to RAM. This second type of memory is named read-only memory, or ROM (rhymes with Tom). Unlike RAM chips, ROM chips have software (program instructions) permanently etched into their circuitry. For this reason, ROM is often referred to as firmware-because it's kind of halfway between hardware and software.

Step 5: RAM Versus ROM



Both RAM and ROM allow random access. If the point is to distinguish RAM from ROM, then RAM would more properly be called read/write memory, meaning that you can both retrieve (read) information from RAM, and record (write) information to it. In contrast, with read-only memory (ROM), instructions are frozen into the circuitry. The feature that sets RAM apart from ROM is its changeability: the fact that you can alter its contents at will.

Step 6: Short-Term and Long-Term Memory

The other difference between RAM and ROM is how long their memories last. RAM is short-term memory; it forgets everything it knows as soon as you turn off your computer. ROM is long-term memory; it remembers everything it has ever known as long as it lives. It's the elephant of the memory kingdom.

Step 7: RAM Stores Part of the OS

In personal computers, ROM is generally used to store some part of the operating system. In IBM-type PCs, only a small part of the operating system is stored in ROM-just enough to get the hardware up and running and to tell the CPU how to locate and load the rest of the operating system from disk.

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